REMARKS/ARGUMENTS

1. Claims 1-6 and 8-15 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,731,696 to Himes et al.

Response:

Claim 1 has been amended to overcome the above rejection. Specifically, claim 1 now includes an additional limitation regarding "the first isolation layer covering a portion of the first electrode in the third region and the substrate in the second region, **but not covering the first electrode in the first region**". The above limitation is supported by the specification, for instance in Fig.6, and is included in order to further define the structural considerations given to the claimed invention and no new matter is introduced.

Himes taught a three plate integrated circuit capacitor comprising a substrate 10, a passivating oxide layer 11, a silicide layer 12', a dielectric oxide 13', and a second silicide plate 15' overlying the oxide layer 13' and being in turn overcoated with a second oxide layer 16' which is made to duplicate the oxide layer 13'. At this point, via holes 19 and 20 are photolithographically etched as shown in Fig. 7. The via hole 19 extends through the oxide layer 16' to expose the silicide layer 15'. The via hole 20 extends through the oxide layers 13' and 16' to expose the silicide layer 12' (Figs. 4-7, column 3, lines 27-46).

The examiner has indicated that the substrate 10 of Himes has a first region, a second region, and a third region defined on the surface thereof as set forth in page 2 of the detailed action. The examiner also indicated that the silicide layer 12' is disposed on the substrate 10 in the first and third regions, the dielectric oxide layer 13' is disposed on the silicide layer 12' and covering portion of the silicide layer 12' and the substrate 10, and the second silicide layer 15' is disposed on the

dielectric oxide layer 13' and covering the dielectric layer 13' in the third region and covering the substrate 10 in the second region. However, it is noteworthy that **Himes' oxide layer 13' is disposed on the silicide layer 12' in both of the first and the third regions while the first isolation layer of the present application covers the first electrode in the third region and the substrate in the second region, but the first isolation layer does not cover the first electrode in the first region.**

Based on this structural difference, the applicant believes the present application is patentably different from Himes' three plate integrated circuit capacitor. Therefore reconsideration of claim 1 is politely requested.

Claim 11 has been amended to overcome the above rejection. Specifically, claim 11 now includes an additional limitation regarding "a dielectric layer covering a portion of the first polysilicon layer in the third region and the substrate in the second region, but not covering the first polysilicon layer in the first region". The above limitation is supported by the specification, for instance in Fig.6, and is included in order to further define the structural considerations given to the claimed invention and no new matter is introduced.

As mentioned above, Himes' oxide layer 13' is disposed on the silicide layer 12' in both of the first and the third regions while the first dielectric layer of the present application covers the first polysilicon layer in the third region but not the first region. Therefore the applicant asserts that the present application is patentably different from Himes' three plate integrated circuit capacitor. Reconsideration of claim 11 is respectfully requested.

Claim 2 is dependent on the amended claim 1 and should be allowed if the amended claim 1 is allowed. Reconsideration of claim 2 is

therefore requested.

Claim 3 recites that the capacitor further comprises a first contact plug located in the second isolation layer and electrically connected to the first electrode. Because Himes' dielectric oxide layer 13' is entirely disposed on the silicide layer 12' in the process, *the via hole 20 is photolithographically etched and extends through oxide layers 13' and 16' (column 3, lines 40-46)*, which means **the via hole 20 of Himes is located in both of the dielectric oxide layer 13' and the second oxide layer 16'**. Therefore the applicant asserts that the present application is distinctly different from Himes. Reconsideration of claim 3 is respectively requested. In addition, claim 12 is dependent on the amended claim 11 and should be allowed if the amended claim 11 is allowed. Reconsideration of claim 12 is politely requested.

Claims 4 and 13 are respectively dependent on claim 3 and 12 and should be allowed if claims 3 and 12 are allowed. Reconsideration of claims 4 and 13 is therefore requested.

Claims 5 and 14 are respectively dependent on claims 2 and 11 and should be allowed if claims 2 and 11 are allowed. Reconsideration of claims 5 and 14 is therefore requested.

Claims 6 and 15 are respectively dependent on claims 5 and 14 and should be allowed if claims 5 and 14 are allowed. Reconsideration of claims 6 and 15 is therefore requested.

Claims 8-10 are dependent on the amended claim 1 and should be allowed if the amended claim 1 is allowed. Reconsideration of claims 8-10 is therefore requested.

2. Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Himes et al. as applied to claims 1 and 11 above, and further in view of US Patent No. 5,769, 887 to Ito et al.

Response:

Claims 7 and 16 are respectively dependent on the amended claims 1 and 11 and should be allowed if the amended claims 1 and 11 are allowed. Reconsideration of claims 7 and 16 is therefore requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/ Winston Hsu / Date: July 3, 2006

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)